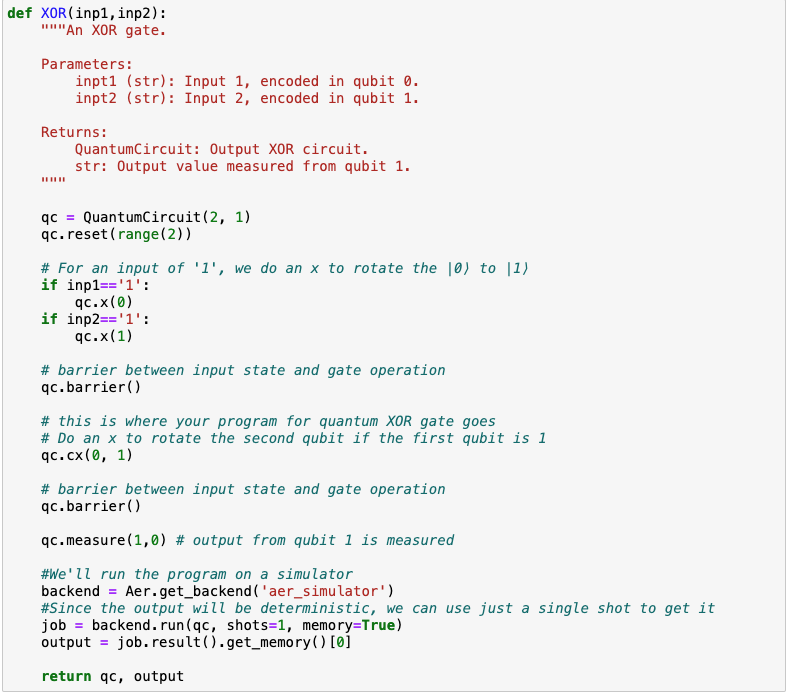
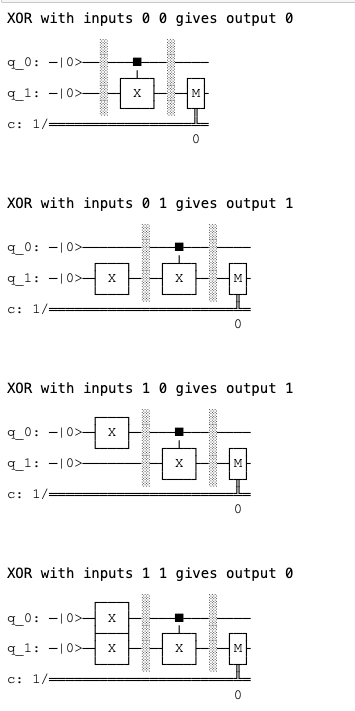
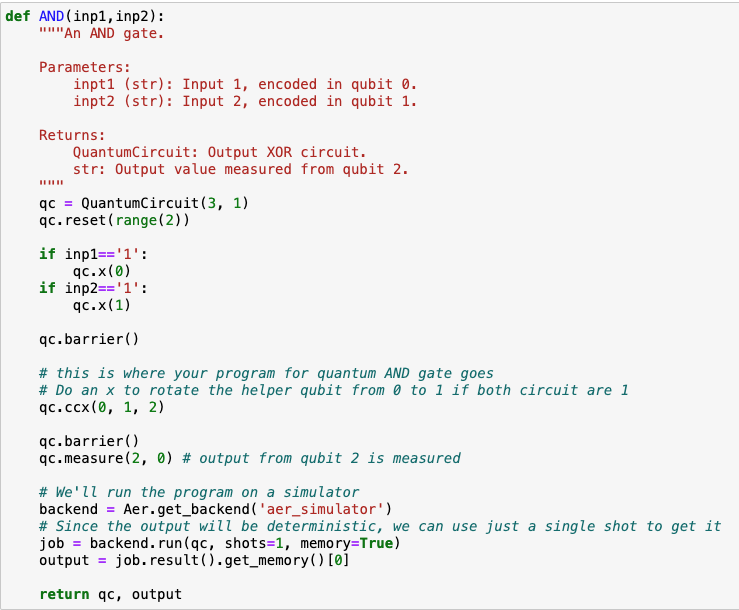
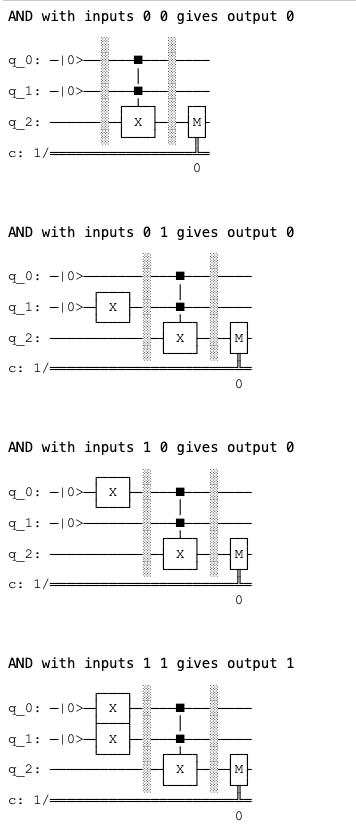
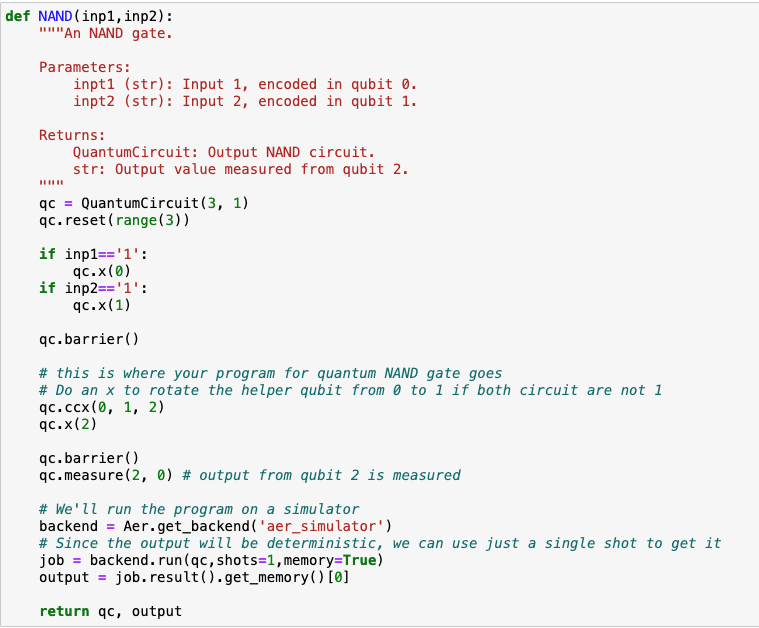
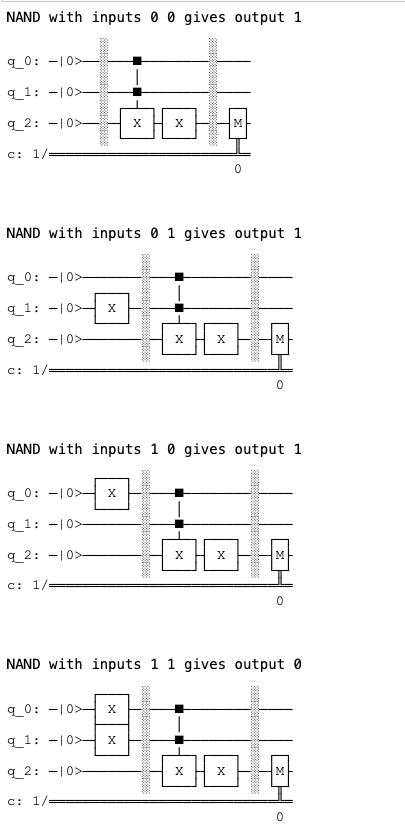
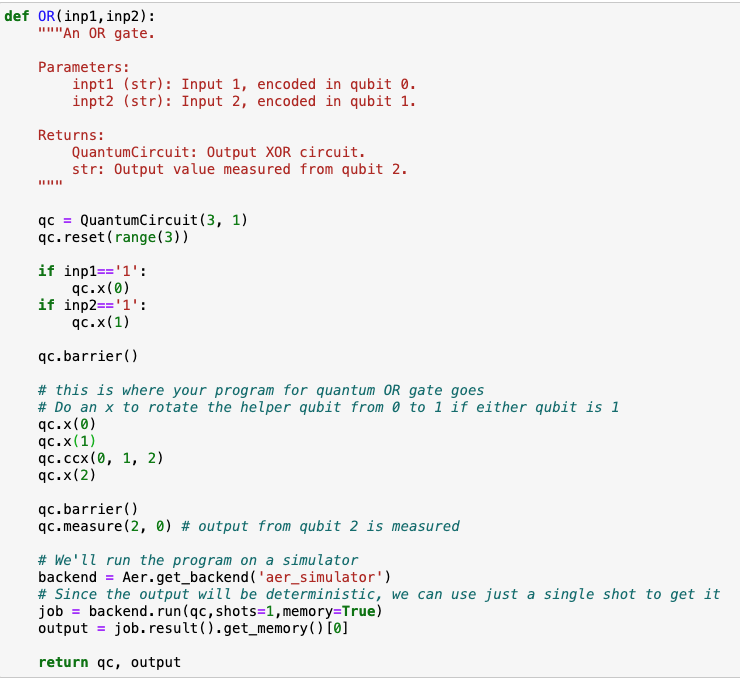
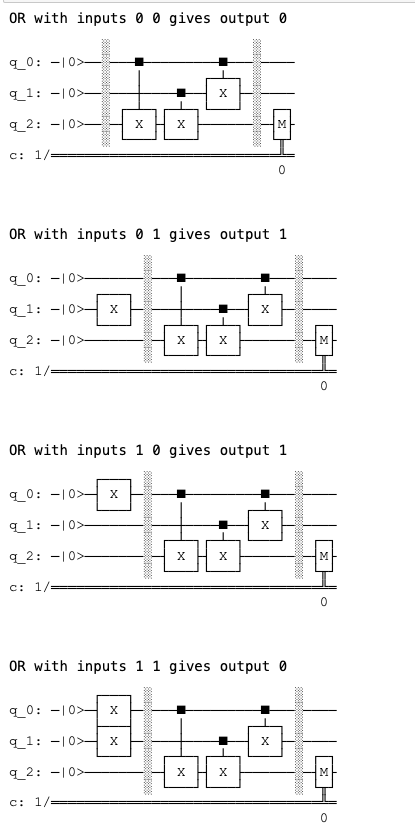
Qiskit Lab 1: Quantum Circuits

In the Qiskit book, Lab 1 is called Quantum Circuits and it focuses on implementing classical

logic gates with quantum circuits. Do the lab plus the additional task below and submit the

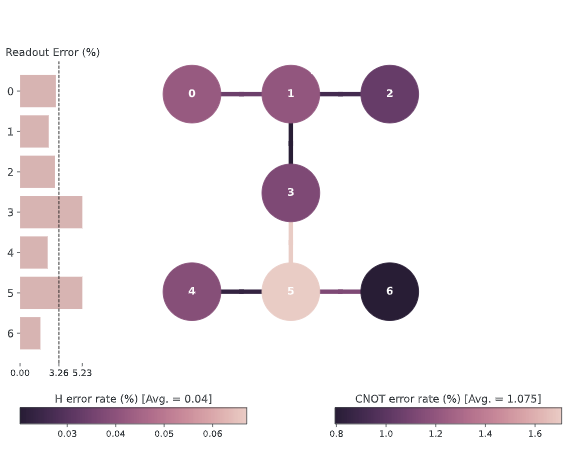
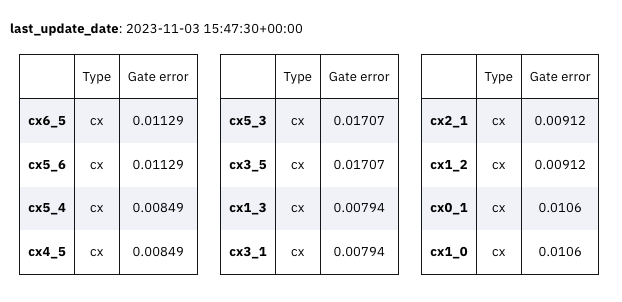
following.

* In Part 1, show your code and circuit diagrams for XOR, AND, NAND, OR.
  + XOR
  + AND
  + NAND
  + OR
* In Part 2:
  + In Step 2, show your three-qubit initial layout and describe the reason for your choice.

The three-qubit initial layout I used is layout = [2, 3, 1].

The following image is the error map for the system ‘ibm\_nairobi’ . In this image, we can observe the error distribution between the qubits. Since most of the gates in the transpiled AND gate are CNOT, we should decide on the three-qubit initial layout based on the CNOT error rate between the qubits. We can find out that the “physical” qubit Q1 is the qubit that has a low CNOT error rate with its neighbor qubits Q2 and Q3, so Q1 can be mapped to the target qubit, and Q2 and Q3 can be mapped to the controlled qubit in the quantum circuit.

Therefore, I put 2 and 3 as the first two elements which represent the “physical” qubits that the two controlled qubits (inp1 and inp2) will map to, and put 1 as the third element which represents the “physical” qubit that the target qubit will map to.





Output of Step 2:

* + In Step 3, explain the reasons for the dissimilarity of the circuits. Describe the relations between the property of the circuit and the accuracy of the outcomes.

Dissimilarity: From these four circuits, we can see that the difference between them lies in their input, the number of nonlocal gates in the circuit, and the circuit depth. The dissimilarity is because each circuit addresses a unique input, resulting in a different arrangement of the gates. The arrangement of gates can significantly impact the circuit depth and the number of nonlocal gates. For example, in the case of input 01, its circuit has a unique input 01, so it has a different gate arrangement than other inputs’ and it also makes the number of nonlocal gates more than other inputs’.

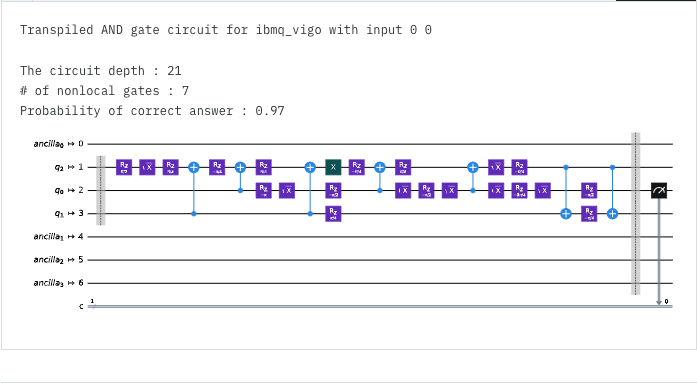
Relations between the property of the circuit and the accuracy of the outcomes:

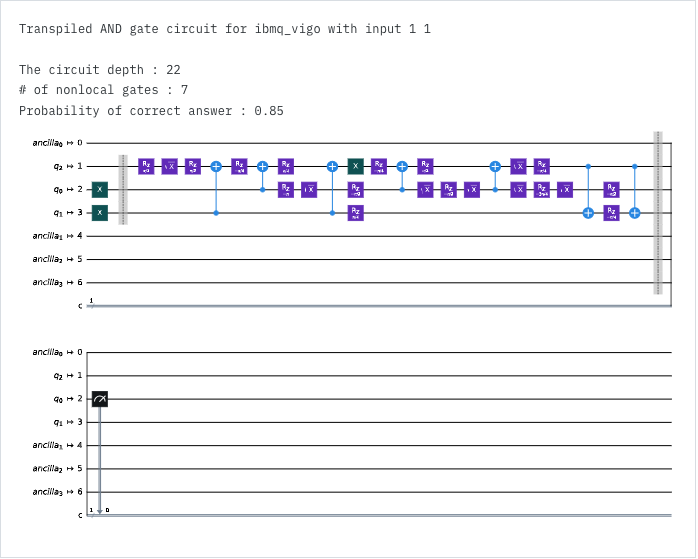
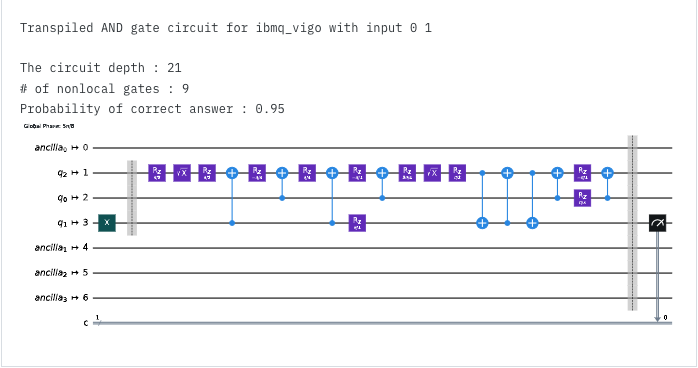
The properties of the circuit are “the circuit depth” and “# of nonlocal gates”. The circuit depth is proportional to the number of gates in a circuit and corresponds to the runtime of the circuit on hardware, so it doesn’t make much impact on the accuracy of the outcomes. Another property is the number of nonlocal gates. In this case, the only nonlocal gate is the CNOT gate. CNOT gates are the most expensive gates to perform and have different gate error rates depending on the controlled qubit and the target qubit, so it will affect the accuracy of the outcomes.

Examples: The CNOT gate will rotate the target qubit only if the controlled qubit is 0. In the case of input 00, the controlled qubit is 0 and it won’t rotate the target qubit, so the error generated by the CNOT gate won’t have a significant impact on the accuracy of the outcomes of this circuit. However, in the case of input 11, the controlled qubit is 1 and it will rotate the target qubit, so the CNOT gate is literally working, and the probability of error generated by the CNOT gate would be much larger. By comparing the result between input 00 and input 11, we can observe that the probability of correct answer for input 11 is much lower than the probability for input 00 which proves my point.



Output of Step 3:



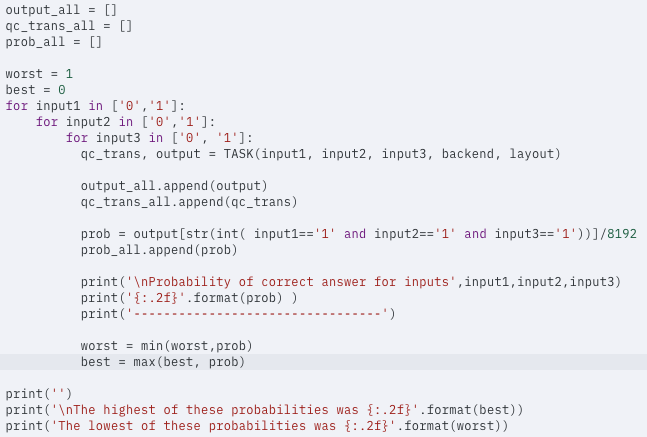


* Additional task:
  + Do Part 2 again, but this time for the logical expression

(x AND y) OR z

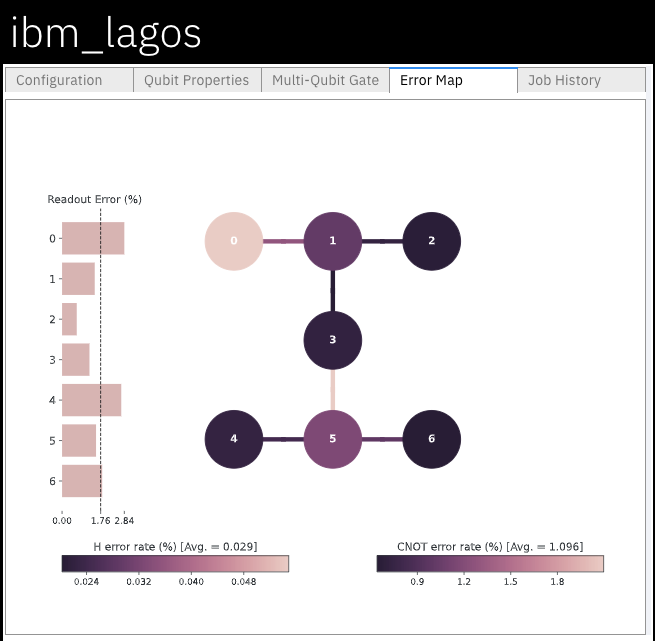
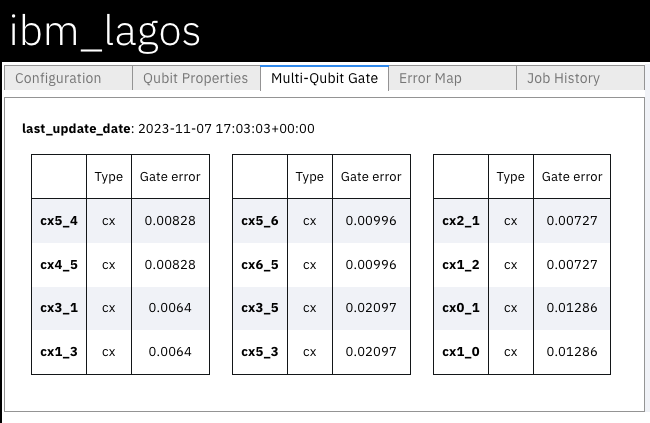
where x,y,z are Boolean variables that you will represent as three qubits. In Step 2, show your qubit initial layout for all the qubits you use and describe the reason for your choice. In Step 3, list the accuracy of the outcome for each circuit, and list the maximum difference across those accuracies.

Step 2:

 Code for the logical expression:

The five-qubit initial layout I used is layout = [4, 6, 1, 5, 3].

The following image is the error map for the system ‘ibm\_lagos’ . Since most of the gates we will use for the logical expression are also CNOT, we should decide on the five-qubit initial layout based on the CNOT error rate between the qubits.

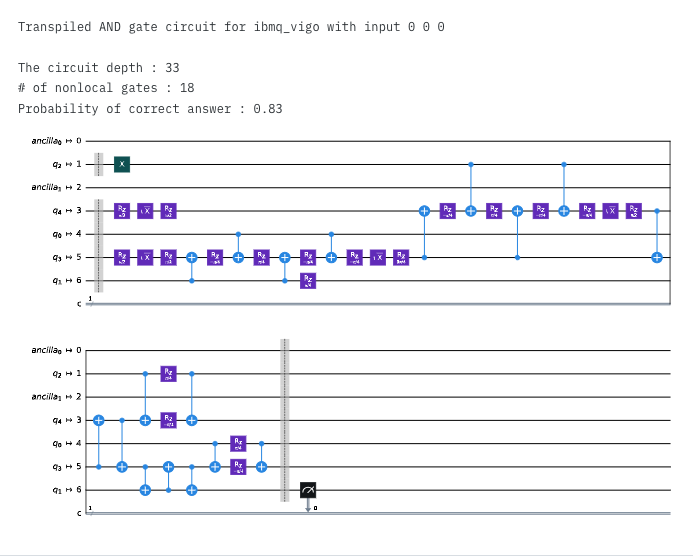


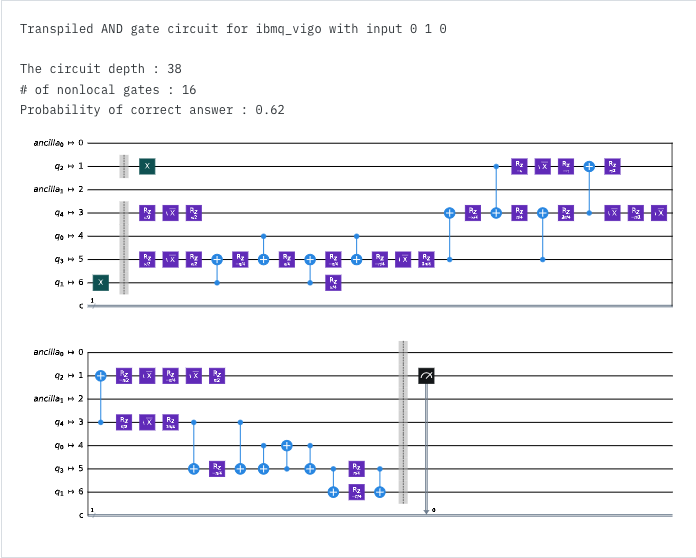
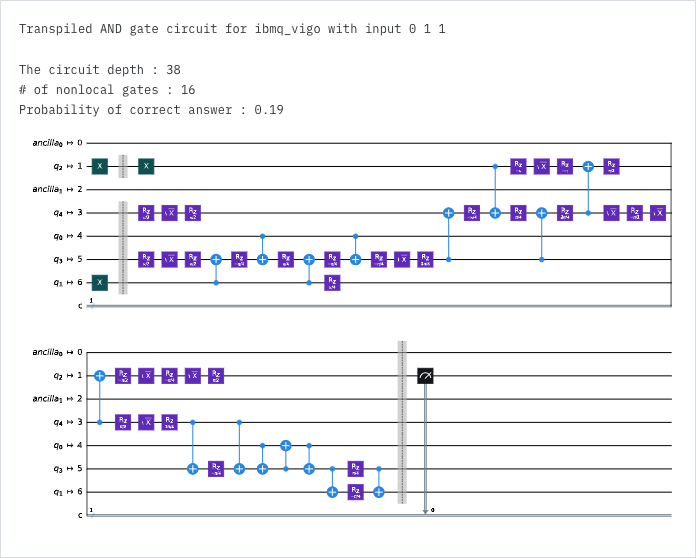
First Toffoli gate: we can find out that the “physical” qubit Q5 is the qubit that has a low CNOT error rate with its neighbor qubits Q4 and Q6, so Q5 can be mapped to the target qubit, and Q4 and Q6 can be mapped to the controlled qubits for the first CCNOT gate. Therefore, I put 4 and 6 as the first two elements which represent the “physical” qubits that the two controlled qubits (inp1 and inp2) will map to, and put 5 as the fourth element which represents the “physical” qubit that the target qubit will map to.

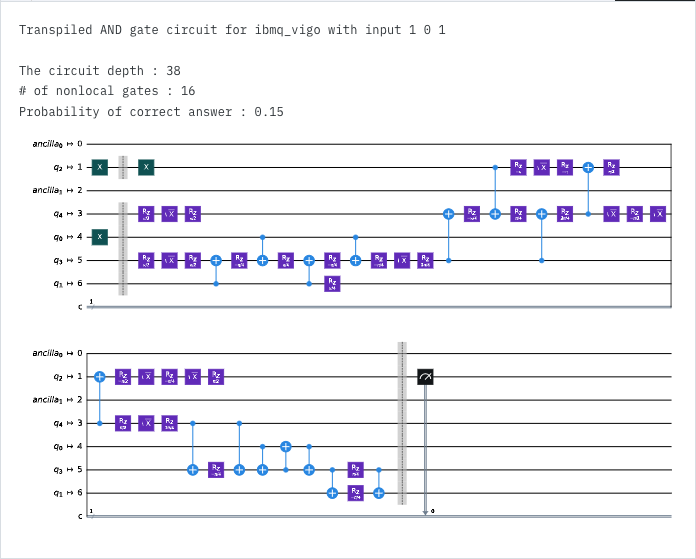
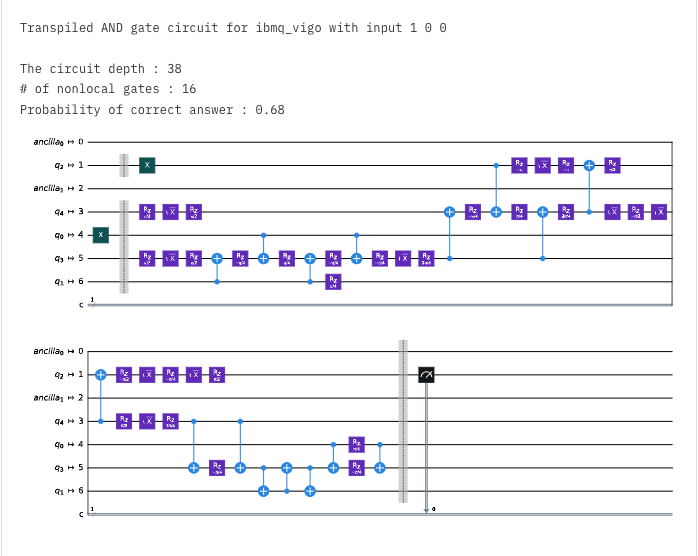
Second Toffoli gate: Since Q5 must be one of the controlled qubits, Q3 must be the target qubit which is the only qubit with the neighbor Q5 besides Q4 and Q6. Q1 is another neighbor of Q3, so it should be another controlled qubit. Therefore, I put 1 as the third element which represents the “physical” qubit (inp3) that one of the controlled qubits will map to, and put 3 as the last element which represents the “physical” qubit that the target qubit will map to and also the measured output.

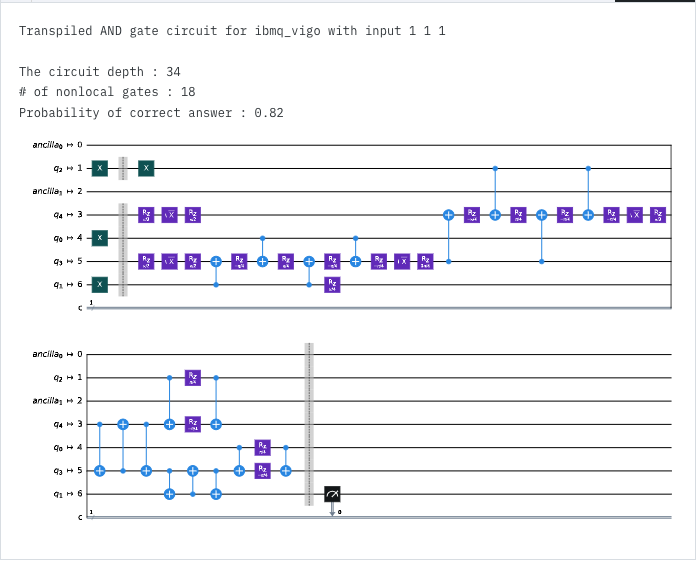
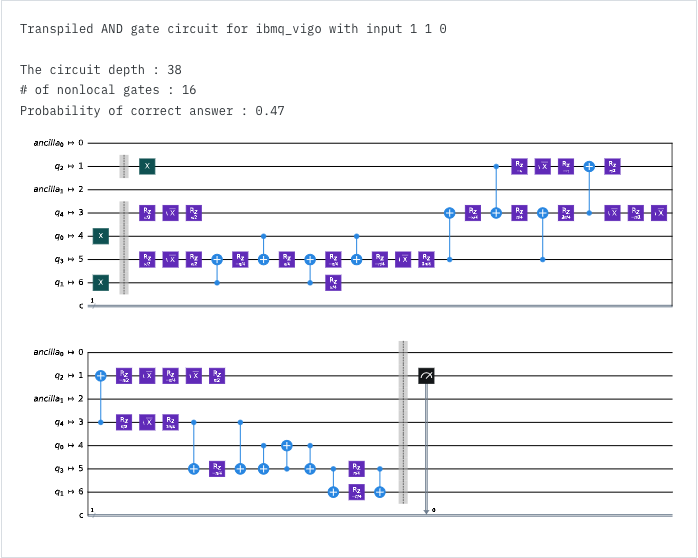
Step 3:

The accuracy of the outcome for each circuit:

000: 0.83 001: 0.13

010: 0.62 011: 0.19

100: 0.68 101: 0.15

110: 0.47 111: 0.82

The maximum difference across those accuracies:

Max = 0.83, Min = 0.13

The maximum difference across those accuracies = Max – Min = 0.83 – 0.13 = 0.7